

# Synchronous Counter Design—Altera Graphic Design Editor, Simulation, and eSOC Board Programming

## Objective

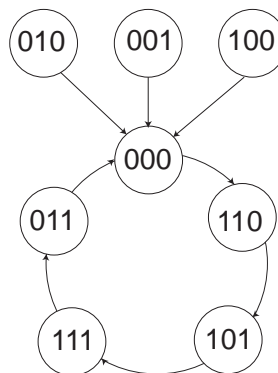
The objective of this experiment is to illustrate the techniques required to design a synchronous counter that counts in an arbitrary sequence, to describe the design using the Altera MAX+plus II Graphic Editor, to simulate it using the Simulator, and to download the design to the CPLD chip to verify its operation.

## Materials Required

PC with Altera MAX+plus II Software  
Function Generator  
DeVry University eSOC Board with parallel cable and power module

## Experimental Procedure

The counter to be designed in this experiment is a synchronous counter that counts in a non-binary sequence as illustrated by the state transition diagram illustrated below:



The counter illustrated is called a self-starting counter because if the counter should happen to start in one of the three states that are not part of the desired sequence (010, 001, and 100), the counter will enter the desired sequence on the first clock edge that occurs after power is applied. If electrical noise should cause the counter to enter one of the unused states, the counter will again enter the desired sequence on the next active clock edge.

The counter will be designed with J-K flip-flops. The operation of a J-K flip-flop may be described by a J-K flip-flop transition table as given below:

Transition	J	K
0 → 0	0	x
0 → 1	1	x
1 → 0	x	1
1 → 1	x	0

The J-K flip-flop transition table illustrates the signal levels required on the J and K inputs to cause a given transition to occur. An entry of x indicates that the input is a don't care and can be either a logical 1 or a logical 0.

The state transition diagram for the counter may be combined with the J-K flip-flop transition table to create a circuit excitation table as illustrated below:

Present State			Next State								
C	B	A	C	B	A	$J_C$	$K_C$	$J_B$	$K_B$	$J_A$	$K_A$
0	0	0	1	1	0	1	x	1	x	0	x
0	0	1	0	0	0	0	x	0	x	x	1
0	1	0	0	0	0	0	x	x	1	0	x
0	1	1	0	0	0	0	x	x	1	x	1
1	0	0	0	0	0	x	1	0	x	0	x
1	0	1	1	1	1	x	0	1	x	x	0
1	1	0	1	0	1	x	0	x	1	1	x
1	1	1	0	1	1	x	1	x	0	x	0

The circuit excitation table illustrates the required J and K inputs for each desired counter transition. The signals that drive the J and K flip-flop inputs are derived from the present state of the flip-flops (C, B, and A) and additional combinational logic. The combinational logic may be designed from Karnaugh Maps (K-Maps) derived from the circuit excitation table. The Karnaugh Maps for our counter design and the resulting Boolean equations are illustrated below:

	C	0	1
BA	00	1	x
	01	0	x
	11	0	x
	10	0	x

$J_C = \bar{A}\bar{B}$

	C	0	1
BA	00	x	1
	01	x	0
	11	x	1
	10	x	0

$K_C = \bar{A}\bar{B} + A\bar{B}$

	C	0	1
BA	00	1	0
	01	0	1
	11	x	x
	10	x	x

$J_B = \bar{A}\bar{C} + AC$

	C	0	1
BA	00	x	x
	01	x	x
	11	1	0
	10	1	1

$K_B = \bar{A} + \bar{C}$

	C	0	1
BA	00	0	0
	01	x	x
	11	x	x
	10	0	1

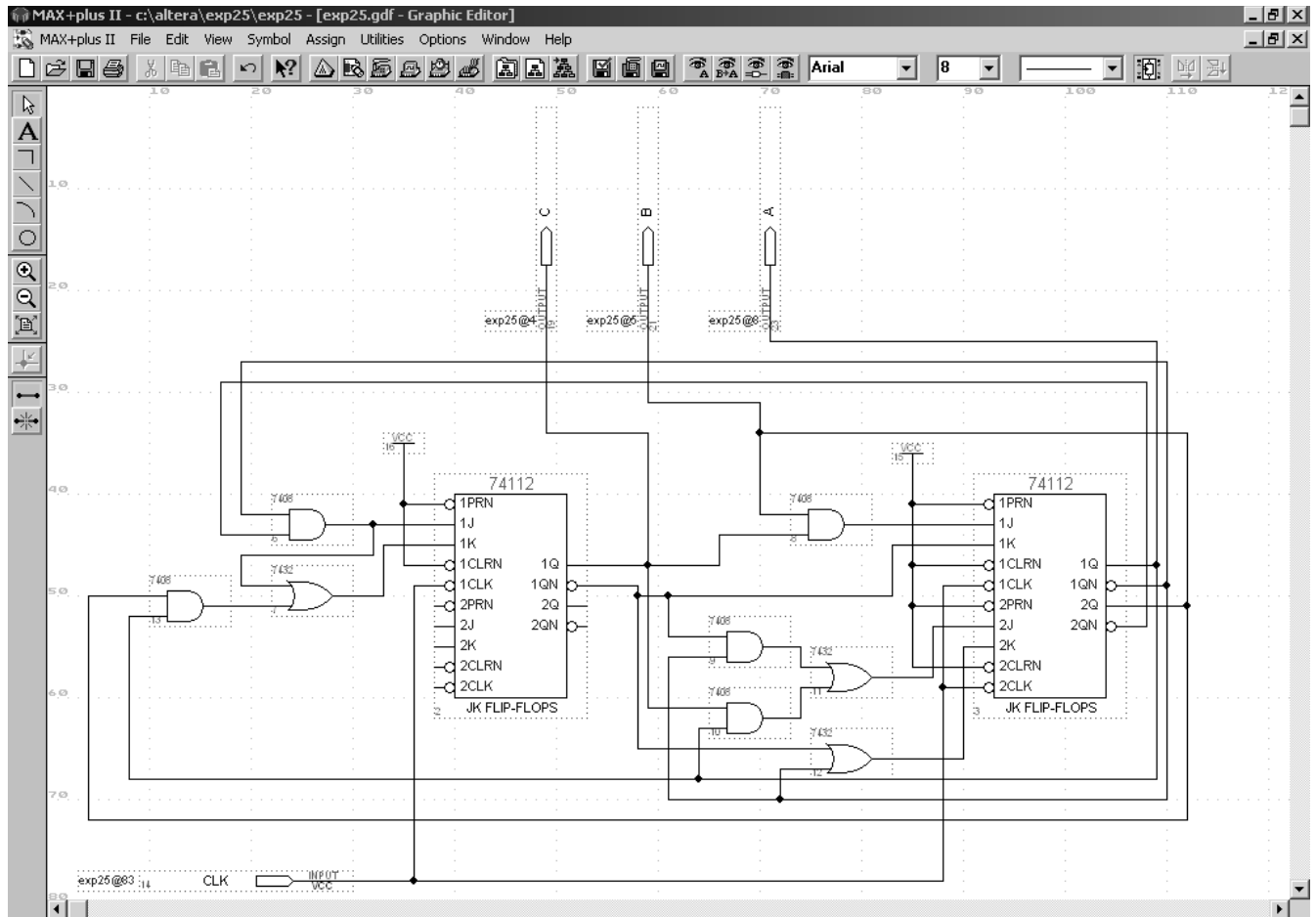
$J_A = BC$

	C	0	1
BA	00	x	x
	01	1	0
	11	1	0
	10	x	x

$K_A = \bar{C}$

The above Boolean equations may be used to design the desired synchronous counter.

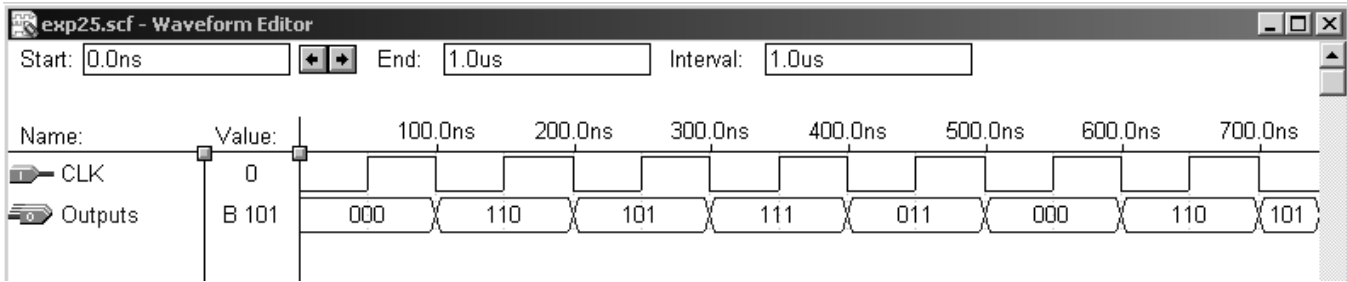
Start MAX+plus II and the Graphic Editor and create the counter circuit illustrated on the next page using 74112 J-K flip-flops, 7408 AND gates, and 7432 OR gates.



Save your Graphic Editor file as p:\altera\exp25\exp25.gdf and change the project name to the name of the current file. Assign the device to the EPM7128SLC84-15. Assign the CLK input to pin 83, the C output to pin 4, the B output to pin 5, and the A output to pin 8.

Compile your design with the Functional SNF Extractor option selected under the Processing menu item.

Start the Waveform Editor and save your file as p:\altera\exp25\exp25.scf. Select CLK, C, B, and A under Enter Nodes from SNF under the Node menu item. Overwrite the clk input with a Clock waveform. Group the flip-flop outputs with the name Outputs under the Node menu item, start the Simulator, and simulate your design. The Waveform Editor output should appear as illustrated on the next page.



Note that the counter counts in the desired non-binary sequence and repeats. Since we disabled the asynchronous preset and clear inputs in our design, we are not able to demonstrate via simulation that the unused states transition to state 000 (which is in the desired sequence) on the first clock edge that occurs.

Recompile your file with the Timing SNF Extractor option selected under the Processing menu item.

Ensure that the parallel cable between your eSOC board and the computer running the Altera software is connected, and likewise that the power module is connected to the board. Ensure that all of the toggle switch enable slide switches are in their off (down) position. Click on the Programmer icon at the top of the workspace, ensure that the Hardware Setup is set to a hardware type of ByteBlaster(MV) and LPT1 under the Options menu item, and then program the CPLD chip on your eSOC board.

After the programming is complete, remove the jumper at JP1 at the top of your eSOC board to allow the user to apply an external clock to CPLD pin 83. The external clock signal (from a function generator) is connected to pin 5 of the connector block J14 at the bottom of your eSOC Board (the eight pins on this connector block are numbered from 1 to 8 with 1 on the left). The ground for the external clock is connected to either pin 7 or pin 8 of J14. The external clock and its ground may alternatively be connected to the marked screw terminals at J1 at the lower right of the eSOC Board. Set the function generator clock frequency to approximately 1.0 Hz and verify that the counter counts in the desired non-binary sequence.

## Report

A report, written in accordance with the specifications provided by your instructor will be required for this experiment by the announced due date.